WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a single or a plurality of memory cell arrays; and

erase means,

wherein:

the memory cell array is configured such that a plurality of nonvolatile memory cells each comprising a variable resistor element for storing information through variations in electric resistance are arranged in each of a row direction and a column direction, and a plurality of word lines and a plurality of bit lines are arranged along the row direction and the column direction, respectively, to select a predetermined memory cell or memory cells from the plurality of memory cells;

the memory cells are arranged such that one end sides of the variable resistor elements are individually connected to drains of selection transistors, the other end sides of the variable resistor elements or sources of the selection transistors are commonly connected to the bit lines along the column direction, the others thereof are commonly connected to the source line, and gates of the selection transistors are commonly connected to the word lines along the row direction; and

the erase means is configured to apply voltage individually to each of the word lines, the bit cells, and the source line that are connected to the memory cell array under predetermined application conditions, to set the electric resistances of the variable resistor elements in individual erase-target memory cells in the memory cell array to a predetermined erased state, and to thereby render the information in the memory cells to be

erasable; and concurrently, the erase means executes the erase by switching between a batch-erase mode and an individual-erase mode depending on the voltage application conditions in at least one of the memory cell arrays, wherein in the batch-erase mode the erase means performs batch erase of all the memory cells in the memory cell array, and in the individual-erase mode the erase means performs individual erase of a part of the memory cells in the memory cell array.

2. The semiconductor memory device according to claim 1, wherein the application conditions of the batch-erase mode and the individual-erase mode are voltage values to be applied to each of the word lines, the bit lines, and the source line.

3. The semiconductor memory device according to claim 1, wherein in the batch-erase mode, for all the memory cells in the memory cell array, the erase means performs operation such that after voltage application is performed under the application condition of the batch-erase mode, a determination is performed whether the individual memory cells have been erased; and if all the memory cells are erased in units of the word line in the row direction, the operation terminates the voltage application in progress under the application condition of the batch-erase mode; and for memory cells not having undergone the erase of all the memory cells in units of the word line in the row direction, the voltage application under the application condition of the batch-erase mode and the determination are iterated for the word lines until all the memory cells are erased in units of the word line in the row direction.

4. The semiconductor memory device according to claim 3, comprising

program means for performing operation such that voltages is applied individually under a predetermined application condition to each of the word lines, the bit lines, and the source line that are to be connected to program-target memory cells in the memory cell array, the electric resistances of the variable resistor elements in the program-target memory cells are set to a predetermined programmed state, and the information are programmed into the individual memory cells, wherein in the batch-erase mode, before the erase means applies the voltage under the application condition of the batch-erase mode to all the memory cells in the memory cell array, the program means performs a program operation so that the electric resistances of the variable resistor elements are set consistent to a predetermined programmed state for all the memory cells.

5. The semiconductor memory device according to claim 1, wherein in the individual-erase mode, for an erase-target memory cell in the memory cell array, the erase means performs operation such that after voltage application is performed under the application condition of the individual-erase mode, a determination is performed whether the memory cell has been erased; for the memory cell erased, the operation terminates the voltage application in progress under the application condition of the individual-erase mode to at least one of the word line and the bit line connected to the memory cell erased; and for the memory cell not erased, the voltage application in the application condition of the individual-erase mode and the determination are iterated until the memory cell is erased in units of the memory cell.

6. A semiconductor memory device comprising:

a plurality of memory cell arrays; and

erase means,

wherein:

the memory cell array is configured such that a plurality of nonvolatile memory cells each comprising a variable resistor element for storing information through variations in electric resistance are arranged in each of a row direction and a column direction, and a plurality of word lines and a plurality of bit lines are arranged along each of the row direction and column direction, respectively, to select a predetermined memory cell or memory cells from the plurality of memory cells;

the memory cells are arranged such that one end sides of the variable resistor elements are individually connected to drains of selection transistors, the other end sides of the variable resistor elements or sources of the selection transistors are commonly connected to the bit lines along the column direction, the others thereof are commonly connected to the source line, and gates of the selection transistors are commonly connected to the word lines along the row direction; and

the erase means is configured to apply voltage individually to each of the word lines, the bit cells, and the source line that are connected to the memory cell array under predetermined application conditions, to set the electric resistances of the variable resistor elements in individual erase-target memory cells in the memory cell array to a predetermined erased state, and to thereby render the information in the memory cells to be erasable;

the erase means is configured such that for at least one of the memory cell

arrays, the erase means renders all the memory cells in the memory cell array to be erasable in batch by setting the application condition of the voltage to the application condition of the batch-erase mode; and the erase means is configured such that for at least other one of the memory cell arrays, the erase means renders a part of the memory cells in the memory cell array to be individually erasable by setting the application condition of the voltage to the application condition of the individual-erase mode.

7. The semiconductor memory device according to claim 6, wherein the application conditions of the batch-erase mode and the individual-erase mode are voltage values to be applied to each of the word lines, the bit lines, and the source line.

8. The semiconductor memory device according to claim 6, wherein in the batch-erase mode, for all the memory cells in the memory cell array, the erase means performs operation such that after voltage application is performed under the application condition of the batch-erase mode, a determination is performed whether the individual memory cells have been erased; and if all the memory cells are erased in units of the word line in the row direction, the operation terminates the voltage application in progress under the application condition of the batch-erase mode; and for memory cells not having undergone the erase of all the memory cells in units of the word line in the row direction, the voltage application under the application condition of the batch-erase mode and the determination are iterated for the word lines until all the memory cells are erased in units of the word line in the row direction.

9. The semiconductor memory device according to claim 8, comprising

program means for performing operation such that voltages is applied individually under a predetermined application condition to each of the word lines in the memory cell array, the bit lines, and the source line that are to be connected to program-target memory cells, the electric resistances of the variable resistor elements in the program-target memory cells are set to a predetermined programmed state, and the information are programmed into the individual memory cells, wherein in the batch-erase mode, before the erase means applies the voltage under the application condition of the batch-erase mode to all the memory cells in the memory cell array, the program means performs a program operation so that the electric resistances of the variable resistor elements are set consistent to a predetermined programmed state for all the memory cells.

10. The semiconductor memory device according to claim 6, wherein in the individual-erase mode, for an erase-target memory cell in the memory cell array, the erase means performs operation such that after voltage application is performed under the application condition of the individual-erase mode, a determination is performed whether the memory cell has been erased; for the memory cell erased, the operation terminates the voltage application in progress under the application condition of the individual-erase mode to at least one of the word line and the bit line connected to the memory cell erased; and for the memory cell not erased, the voltage application in the application condition of the individual-erase mode and the determination are iterated until the memory cell is erased in units of the memory cell.

11. An erase method for a memory cell array of a semiconductor

memory device, wherein:

the semiconductor memory device comprises a single or a plurality of memory cell arrays each configured such that a plurality of nonvolatile memory cells each comprising a variable resistor element for storing information through variations in electric resistance are arranged in each of a row direction and a column direction, and a plurality of word lines and a plurality of bit lines are arranged in the row direction and the column direction, respectively, to select a predetermined memory cell or memory cells from the plurality of memory cells;

the memory cells are arranged such that one end sides of the variable resistor elements are individually connected to drains of selection transistors, the other end sides of the variable resistor elements or sources of the selection transistors are commonly connected to the bit lines along the column direction, the others thereof are commonly connected to the source line, and gates of the selection transistors are commonly connected to the word lines along the row direction;

the erase method comprises a batch-erase mode and a individual-erase mode, wherein the batch-erase mode is used to perform batch erase of all the memory cells in the memory cell array in units of the memory cell array, and the individual-erase mode is used to perform individual erase of a part of the memory cells in the memory cell array;

in each the batch-erase mode and the individual-erase mode, the erase method applies voltage individually to each of the word lines, the bit cells, and the source line that are connected to the memory cell array under predetermined application conditions, sets the electric resistances of the

variable resistor elements in individual erase-target memory cells in the memory cell array to a predetermined erased state, and thereby erases the information in the memory cells; and

the application condition of the batch-erase mode and the application condition of the individual-erase mode are different in an application condition at least for one of the word line, the bit line, and the source line.

12. The erase method according to claim 11, wherein in the batch-erase mode, for all the memory cells in the memory cell array, the erase method performs operation such that after voltage application is performed under the application condition of the batch-erase mode, a determination is performed whether the individual memory cells have been erased; and if all the memory cells are erased in units of the word line in the row direction, the operation terminates the voltage application in progress under the application condition of the batch-erase mode; and for memory cells not having undergone the erase of all the memory cells in units of the word line in the row direction, the voltage application under the application condition of the batch-erase mode and the determination are iterated for the word lines until all the memory cells are erased in units of the word line in the row direction.

13. The erase method according to claim 12, wherein in the batch-erase mode, before applying the voltage under the application condition of the batch-erase mode to all the memory cells in the memory cell array, the erase method performs a program operation so that the electric resistances of the variable resistor elements are set consistent to a predetermined programmed state for all the memory cells.

14. The erase method according to claim 11, wherein in the individual-erase mode, for an erase-target memory cell in the memory cell array, the erase method performs operation such that after voltage application is performed under the application condition of the individual-erase mode, a determination is performed whether the memory cell has been erased; for the memory cell erased, the operation terminates the voltage application in progress under the application condition of the individual-erase mode to at least one of the word line and the bit line connected to the memory cell erased; and for the memory cell not erased, the voltage application in the application condition of the individual-erase mode and the determination are iterated until the memory cell is erased in units of the memory cell.